UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,133	05/19/2006	Kohji Yoshii	R2184.0496/P496	9224

24998 7590 01/21/2010

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
ABBASZADEH, JAWEED A	
ART UNIT	PAPER NUMBER
2115	
MAIL DATE	DELIVERY MODE
01/21/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,133	YOSHII, KOHJI	
	Examiner	Art Unit	
	JAWEED A. ABBASZADEH	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-10 and 12-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-2, 4-10, and 12* is/are allowed.

6)☒ Claim(s) *13-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-2, 4-10, and 12-16 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohout et al. (hereinafter 'Kohout') US 6,969,979 in view of Teraishi US 6,518,848.

As to claim 13, Kohout teaches a method for operating a switching regulator [col. 2, lines 41-45], the method comprising:

a control circuit to stop operating when the standby signal is asserted [col. 7, lines 18-21 and col. 3, lines 16-18]. Kohout does not specifically teach detecting a clock, grounding a determination node when the clock rises, allowing the potential at the determination node to rise above a threshold if the clock does not rise, and asserting a signal if the potential rises above the threshold. Specifically, Kohout teaches low power mode being automatically initiated without the use of expensive external components.

Teraishi is cited to teach a method for detecting a clock signal. Teraishi further teaches detecting a clock signal [col. 3, lines 27-29];

grounding a determination node [Fig. 2, N1] when the clock signal rises [Fig. 2, At t3 and t5 the clock (ck) rises and causes the potential at N1 to go to L which is interpreted as ground;

allowing the potential at the determination node to rise above a threshold level if the clock signal does not rise [col. 5. lines 45-55]; and

asserting a signal if the potential at the determination node rises above the threshold level [col. 5, lines 50-55]. It would have been obvious to one of ordinary skill in the art to have combined the teachings of Kohout and Teraishi because Teraishi provides Kohout an alternate method to determine when a low power mode should be entered. Teraishi provides a method to detect a clock signal and reducing a pattern area of an integrated circuit [col. 3, lines 28-30]. A switching regulator depends on a clock in order to operate and determining if a clock is not running would be an obvious scenario in which a switching regulator should enter a low power mode. Kohout determines if the current is below a certain value to enter low power mode [col. 6, lines 33-35]. Without the clock, a switching regulator would not be able to produce current. Therefore, clock detection would be a more fundamental method to initiate a low power mode in a switching regulator.

As to claim 14, Kohout and Teraishi teach this claim according to the reasoning set forth in claim 13.

As to claim 15, Teraishi teaches the step of grounding the potential at a determination node further comprises:

inverting the clock signal to create an inverted clock signal;

comparing [EOR] the clock signal to the inverted clock signal to determine a period of delay caused by said inverting to create a comparison voltage; and

activating the gate of a transistor with the comparison voltage when the comparison voltage is high to ground the potential at the determination node [col. 5, lines 1-10].

As to claim 16, Teraishi teaches the steps of allowing the potential at the determination node to rise further comprises:

inverting the clock signal to create an inverted clock signal;

comparing [EOR] the clock signal to the inverted clock signal to determine a period of delay caused by said inverting to create a comparison voltage; and

deactivating the gate of a transistor with the comparison voltage when the comparison voltage is low to allow the potential at the determination node to rise [col. 5, lines 45-55].

Allowable Subject Matter

Claim 1-2, 4-10 and 12 are allowed.

Response to Arguments

Applicant's arguments with respect to claim13-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAWEED A. ABBASZADEH whose telephone number is (571)270-1640. The examiner can normally be reached on Mon-Fri: 7:30 a.m.-5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jaweed A Abbaszadeh/
Examiner, Art Unit 2115
1/16/2010

/Thomas Lee/
Supervisory Patent Examiner, Art Unit 2115